

IN THE CLAIMS

1. (Canceled)
2. (Original) An integrated circuit field effect transistor comprising:
 - a source and a drain separated by a channel supported by a semiconductor substrate;
 - a gate supported by the substrate and extending between the source and drain above the channel; and
 - an insulative amorphous layer of carburized silicon grown on the channel and located between the channel and the gate.
3. (Previously Amended) An integrated circuit memory device supported by a semiconductor substrate, the device comprising:
 - a source and a drain separated by a channel supported by a semiconductor substrate;
 - a floating gate supported by the substrate and extending between the source and drain above the channel;
 - a control gate formed adjacent to and insulated from the floating gate; and
 - an insulative layer of amorphous carburized silicon grown on the channel and located between the channel and the floating gate.
- 4 - 6 (Canceled)
- 7- 19 (Withdrawn)
- 20 - 23 (Canceled)
24. (Previously Amended) A transistor comprising:
 - a source region in a substrate;
 - a drain region in the substrate;
 - a channel region between the source region and the drain region in the substrate; and

a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

25. (Previously Added) The transistor of claim 24 wherein the gate comprises a floating gate.

26. (Previously Added) The transistor of claim 25, further comprising a control gate separated from the floating gate.

GI 27. (Previously Added) The transistor of claim 24 wherein the substrate comprises a semiconductor surface layer on an underlying insulating portion.

28. (Previously Added) The transistor of claim 24 wherein the substrate comprises a doped silicon semiconductor substrate.

29 - 40 (Canceled)

41. (Previously Amended) The integrated circuit field effect transistor of claim 2 wherein:
the semiconductor substrate comprises a p-type silicon substrate;
the source comprises an n⁺-type source region in the substrate;
the drain comprises an n⁺-type drain region in the substrate;
the channel comprises a channel region in the substrate between the source region and the drain region; and

the amorphous layer of carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

42. (Previously Amended) The integrated circuit field effect transistor of claim 2 wherein:
the semiconductor substrate comprises a p-type silicon substrate;
the source comprises an n⁺-type source region in the substrate;
the drain comprises an n⁺-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region;

the gate comprises a floating gate isolated from the channel region by the amorphous layer of carburized silicon;

the amorphous layer of carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and

further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

43. (Previously Amended) The device of claim 3 wherein:

the semiconductor substrate comprises a p-type silicon substrate;

the source comprises an n+-type source region in the substrate;

the drain comprises an n+-type drain region in the substrate;

the channel comprises a channel region in the substrate between the source region and the drain region;

the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

44. (Previously Amended) The transistor of claim 24 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region in the substrate;

the drain region comprises an n+-type drain region in the substrate; and

the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

45. (Previously Amended) A transistor comprising:

an n+-type source region in a p-type silicon substrate;

an n+-type drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and
a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

46. (Previously Amended) A transistor comprising:
a source region in a substrate;
a drain region in the substrate;
a channel region between the source region and the drain region in the substrate; and
a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

47. (Previously Amended) The transistor of claim 46 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n⁺-type source region in the substrate;
the drain region comprises an n⁺-type drain region in the substrate;
the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas; and
further comprising a polysilicon control gate separated from the floating gate by a layer of insulating material.

48. (Previously Amended) A transistor comprising:
an n⁺-type source region in a p-type silicon substrate;
an n⁺-type drain region in the substrate;
a channel region between the source region and the drain region in the substrate;
a floating gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate; and
a polysilicon control gate separated from the floating gate by a layer of insulating material.

49. (Canceled)

50. (Previously Added) A memory cell comprising:

- a source region in a substrate;
- a drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate;
- a layer of amorphous carburized silicon grown on the substrate between the floating gate and the channel region; and
- a control gate separated from the floating gate.

51. (Previously Amended) The memory cell of claim 50 wherein:

- the substrate comprises a p-type silicon substrate;
- the source region comprises an n⁺-type source region in the substrate;
- the drain region comprises an n⁺-type drain region in the substrate;
- the control gate comprises a polysilicon control gate separated from the floating gate by a layer of insulating material; and
- the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

52. (Previously Amended) A memory cell comprising:

- an n⁺-type source region in a p-type silicon substrate;
- an n⁺-type drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate;
- a layer of amorphous carburized silicon grown on the substrate between the floating gate and the channel region; and
- a polysilicon control gate separated from the floating gate by a layer of insulating material.

53 - 64 (Canceled)

65. (Previously Added) The transistor of claim 45 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

66. (Previously Added) The transistor of claim 48 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

67. (Previously Added) The memory cell of claim 52 wherein the layer of amorphous carburized silicon was grown on the substrate in a microwave-plasma-enhanced chemical vapor deposition chamber in a hydrocarbon containing gas.

68. (Previously Added) A transistor comprising:
a source region in a substrate;
a drain region in the substrate;
a channel region between the source region and the drain region in the substrate;
a floating gate; and
means for separating the floating gate from the channel region.
